MEMORY INTERFACE SYSTEM

This application claims priority from Korean patent application number 03-24781 filed April 18, 2003 that we incorporate herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a semiconductor memory device and, more particularly, to an interface system for a semiconductor memory device.

2. Description of the Related Art

A bus is typically used when two or more signals are routed in parallel over significant distances. The bus will often contain two wires per signal resulting in transmission of a differential signal. The differential signal improves bus speed. Several developments, however, work to adversely affect bus speed. Among them is increased line delay due to increases in line resistance resulting from reductions in line widths and elongations of line lengths. And line delays increase as the separation between differential lines decreases increasing line-to-line capacitance.

One way to improve bus speed is to encode digital data on multiple signal levels and transmit it on a single line. This and other approaches are described in several patents, including U.S. patent number 6,211,698 to Suh and U.S. patents numbers 6,275,067, 6,300,795, 6,320,417, all to Kirsch and others. In all of these cases, however, the devices described suffer from various disadvantages, including lack of implementation flexibility, reduced timing margins, and state discontinuities that lead to decreased speed and increased data errors.

Accordingly, a need remains for an improved interface system for a semiconductor memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features, and advantages of the invention will become more readily apparent from the detailed description of an embodiment that references the following drawings.

Figure 1A is a block diagram of a memory interface embodiment.

Figure 1B is a timing diagram associated with memory interface embodiment shown in Figure 1A.

Figure 2A is a block diagram of a transmitter embodiment.

Figure 2B is a timing diagram associated with the transmitter shown in Figure 2A.

Figures 3A and 3B are timing diagrams of symbol definition embodiments associated with the memory interface shown in Figure 1.

Figure 4A is a block diagram of a receiver embodiment.

Figures 4B-C are block diagrams of the receiver embodiment shown in Figure 4A.

Figure 5 is a timing diagram associated with the transmitter shown in Figures 4A-C.

Figure 6 is a timing diagram associated with the invention embodiment shown in Figure 1.

Figure 7 is a block diagram of an invention embodiment.

Figure 8 is a diagram of the reference voltage associated with the receiver embodiment shown in Figures 4A-C.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1A is a block diagram of an interface system according to an embodiment of the present invention. Referring to Figure 1A, the interface system 100 includes a transmitter 102, a receiver 104, and a transmission line 106. The transmitter 102 receives input signals TX_D1 and TX_D2 and generates multiple bit symbol data D1D2 responsive to first and second transmit clocks TCLK1 and TCLK2, respectively.

The input signals TX_D1 and TX_D2 are, e.g., single bit or two level signals. The symbol data D1D2, on the other hand, is, e.g., a multiple bit or at least three level signal. In one embodiment, the symbol data D1D2 results from superpositioning the input signals TX_D1 and TX_D2. The symbol data D1D2 might, e.g., provide two data bits per bit time. By doing so, the interface 100 increases bandwidth.

In one embodiment, the bit time is half a period of an external clock. A person of reasonable skill in the art should recognize that the bit time might have different periods and vary according to a variety of internal or external clocks.

The transmission line 106 transmits the symbol data D1D2 to the receiver 104. The receiver 104 decodes the symbol data D1D2 to generate output signals RX_D1 and RX_D2

responsive to first and second receive clocks RCLK1 and RCLK2, respectively. The output signals RX_D1 and RX_D2 are, e.g., single bit signals.

Figure 1B is a timing diagram of the invention embodiment shown in Figure 1A. Referring to Figure 1B, the first transmitter and receiver clocks TCLK1 and RCLK1 are synchronized with an external clock CLK. In one embodiment, the second transmitter and receiver clocks TCLK2 and RCLK2 are out of phase relative to the first transmitter and receiver clocks TCLK1 and RCLK1, e.g., 90 degrees out of phase.

Figure 2A is a block diagram of an embodiment of the transmitter 102 shown in Figure 1A. The transmitter 202 includes first and second transmitting circuits 210 and 212 coupled to a superposition node 214. The superposition node 214 is coupled to a transmission line 206. The first transmitting circuit 210 receives the first input signal TX_D1 and generates first transmit signal TX_D1' responsive to the first transmit clock TCLK1. Likewise, the second transmitting circuit 212 receives the second input signal TX_D2 and generates second transmit signal TX_D2' responsive to the second transmit clock TCLK2. The node 214 superpositions first and second transmit signals TX_D1' and TX_D2' to generate and provide the symbol data D1D2 to the transmission line 206. The operation and structure of the first and second transmitting circuits 210 and 212 is well known and disclosed in, e.g., U.S. patent number 6,184,714 to Kirsch that is incorporated herein by reference.

In one embodiment, the input signals TX_D1 and TX_D2 are two level signals. In one embodiment, the symbol data D1D2 is at least a three level signal. This means that the symbol data D1D2 uses at least three voltage levels, e.g., high voltage level H, low voltage level L, and medium voltage level M, to indicate a data state. In one embodiment, the medium voltage level M is an arithmetic average of the high and low voltage levels H and L, respectively.

Figure 2B is a timing diagram of the transmitter 202. The first transmitting circuit 210 transmits the first input signal TX_D1 as the first transmit signal TX_D1' for a bit time A of the transmitter clock TCLK1. In a double data rate device, the first transmitting circuit 210 transmits at both the falling and rising edges of the first transmitter clock TCLK1. The first transmit signal TX_D1' is a version of the first input signal TX_D1 synchronized with the first transmitter clock TCLK1.

The second transmitting circuit 212 transmits the second input signal TX_D2 for a bit time B of the transmitter clock TCLK2. In a double data rate device, the second transmitting

circuit 212 transmits at both the falling and rising edges of the second transmitter clock TCLK2. The second transmitter signal TX_D2' is a version of the second input signal TX_D2 synchronized with the second transmitter clock TCLK2.

The node 214 superpositions the first and second transmit signals TX_D1' and TX_D2' out of phase with each other. In one embodiment, the node 214 superpositions the first and second transmit signals TX_D1' and TX_D2' 90 degrees out of phase with each other. The superposition node 214 generates the symbol data D1D2.

The symbol data D1D2 encodes various states or symbol. A symbol is a unique signal shape in a predetermined unit of time, e.g., bit times A or B. The symbol data D1D2 includes symbol sequences S2-S7-S4-S5-S3-S3-S2-S5-S2 relative to the first transmitter reference clock TCLK1 and sequences S6-S5-S6-S1-S3-S3-S6-S1-S6 relative to the second transmitter reference clock TCLK2.

Figures 3A and 3B are timing diagrams of symbol definition embodiments associated with the memory interface shown in Figure 1. Referring to Figure 3A, the symbol data D1D2 employs two bit data. Because the symbol data D1D2 is created by the superposition of out of phase input signals, one two bit data is a full bit datum of the first input signal TX_D1 and two half bits of TX_D2 relative to bit time A. Relative to bit time B, the symbol data D1D2 includes a full bit datum of the second input signal TX_D2 and two half bits of the first input signal TX_D1.

In one embodiment, the symbol S2 is the superposition of a full bit datum A3 of TX_D1 and the second half bit of B2 and the first half bit of B3 of TX_D2. The first half bit of S2 is a logic high H resulting from the superposition of the first half bit of A3 of TX_D1 and the second half bit of B2. The second half bit of S2 is a logic medium M resulting from the superposition of the second half bit of A3 of the TX_D1 and the first half bit of B3 of TX_D2. The symbol S2, therefore, has an H and M sequence.

The symbol S3 has an H and H sequence. The symbol S5 has an L and M sequence. The symbol S6 has an M and L sequence. The symbol S7 has an L and L sequence.

All symbols have unique signal shapes corresponding to combinations of the first and second input signals TX_D1 and TX_D2 except for symbol S4. Symbol S4 has duality. In a first case, symbol S4 comprises the superposition of TX_D1's full-bit datum A7 and the second half bi of B6 and the first half bit of B7. The data A7 is a logic H and the data B6 and B7 are L. In a second case, the symbol S4 comprises the superposition of TX_D2's full-bit datum C7 and the second half bit of D6 and the first half bit of D7. The data C7 is a logic L

and the data D6 and D7 are logic H. It should be apparent to a person of reasonable skill in the art that the full bit data of symbol S4 is the inversion of the half bit data. Receiver 104 will use this relationship to interpret the symbol S4.

Figure 4A is a block diagram of an embodiment of the receiver 104 shown in Figure 1A. Referring to Figures 1 and 4A, the receiver 404 includes first and second receiving circuits 410 and 420, respectively. The first and second receiving circuits 410 and 420 receive the symbol data D1D2. The first receiving circuit 410 generates the signal RX_D1 by interpreting the symbol data D1D2 responsive to a first receiving clock RCLK1 and RCLK1B. Likewise, the second circuit 420 generates the signal RX_D2 by interpreting the symbol data D1D2 responsive to a second receiving clock RCLK2 and RCLK2B.

The first receiving circuit 410 generates the signals RX_D1_even and RX_D1_odd and provides them to the second receiving circuit 420. The second receiving circuit 420 generates the signals RX_D2_even and RX_D2_odd and provides them to the first receiving circuit 410.

Figure 4B is a block diagram of the first receiving circuit 410 shown in Figure 4A. Referring to Figures 4A-B, the receiver 410 includes a first detector 411 capable of generating the first even and odd data signals RX_D1_even' and RX_D1_odd', respectively, responsive to a medium reference voltage VrefM. An amplifier 411_a compares the symbol data D1D2 to the medium reference voltage VrefM, providing the results of the comparison to integrators 411_b and 411_c and sense circuits 411_d and 411_e. In one embodiment, the amplifier 411_a is a differential amplifier. The integrator 411_b and the sense circuit 411_d operate responsive to the first receiving clock RCLK1. The integrator 411_c and the sense amplifier 411_e operate responsive to a clock RCLK1b. The bit-time integrator 411_b integrates the output of the amplifier 411_a during the high level of the clock RCLK1. The sense circuit 411_d determines and maintains the output of the integrator 411_b during the low level of the clock RCLK1. Likewise, the bit-time integrator 411_c integrates the output of the amplifier 411_a during the high level of the clock RCLK1b. The sense circuit 411_e determines and maintains the output of the integrator 411_c during the low level of the clock RCLK1b. In one embodiment, clock RCLK1 is out of phase relative to clock RCLK1b by, e.g., 180 degrees, as shown in Figure 5.

A second detector 412 is capable of generating first even and odd select signals DATASEL1_e and DATASEL0_o, respectively, responsive to high and low reference voltages VrefH and VrefL. The second detector 412 operates responsive to the clocks

RCLK1_1st and RCLK1_2nd. An amplifier 412_a compares the symbol data D1D2 to the high and low reference voltages VrefH and VrefL providing the results to integrators 412_b to 412_e and sense amplifiers 412_f to 412_i. In one embodiment, the amplifier 412_a is a folded amplifier. When the voltage level of the symbol data D1D2 is between VrefH and VrefL, the output of the pre-amplifier 412_a is a logic high. In all other cases, the output of the amplifier 412_a is a logic low. It should be apparent to a person of reasonable skill in the art that this logic can be reversed and still come within the scope of the present invention.

Integrators 412_b to 412_e and sense circuits 412_f to 412_i operate responsive to clock signals RCLK1_1st, RCLK1_2nd, RCLK1b_1st, and RCLK1b_2nd, the relationship between them being shown in Figure 5. In one embodiment, the integrators 412_b to 412_e are, e.g., half bit time integrators. The sense circuit 411_d determines and maintains the output of the integrator 411_b. The sense circuit 411_e determines and maintains the output of the integrator 411_c. The sense circuits 412_f and 412_g determines and maintains the output of the integrators 412_b and 412_c, respectively. The sense circuits 412_h and 412_i determines and maintains the output of the integrators 412_d and 412_e, respectively.

Logic gates 412_j and 412_k logically manipulate the output of sense amplifiers 412_f and 412_g and 412_h and 412_i, respectively, to generate the first even and odd select signals DATASEL1_e and DATASEL0_o, respectively. The signal DATASEL1 _e is a logic high when the outputs of the sense circuits 412_f and 412_g are logic high. On the other hand, the signal DATASEL1_e is a logic low when the outputs of the sense circuits 412_f or 412_g are low. Likewise, the signal DATASEL1 _o is a logic high when the outputs of the sense circuits 412_h and 412_i are logic high. On the other hand, the signal DATASEL1_o is a logic low when the outputs of the sense circuits 412_h or 412_i are low.

A multiplexer 413 selects between the signals RX_D1_even' and RX_D2_odd responsive to the first even select signal DATASEL1_e. And the multiplexer 413 selects between the signals RX_D1_odd' and RX_D2_even responsive to the first odd select signal DATASEL1_o.

In one embodiment, when the logic value of DATASEL1_e is high, the multiplexer 413_e selects the inverted RX_D2_odd as its output. When the logic value of DATASEL1_e is low, the multiplexer 413_e selects the RX_D1_even' as its output. In one embodiment, when the logic value of DATASEL1 _o is high, the multiplexer 413_o selects the inverted RX_D2_even as its output. When the logic value of DATASEL1_o is low, the multiplexer 413_o selects the RX_D1_odd' as its output.

To achieve double data rate operation, the receiver 410 has an even and an odd data path as is evident from the above description. The even data path includes amplifiers 411_a and 412_a, integrator 411_b (full-bit), integrators 412_b and 412_c (half-bit), sense circuits 411_d, 411_f, and 411_g, and data select circuit 412_j. The odd data path includes amplifiers 411_a and 412_a, integrator 411_c (full-bit), integrators 412_d and 412_e (half-bit), sense circuits 411_e, 411_h, and 411_i, and data select circuit 412_k.

The receiver 410 overlaps the following basic operations: integration and sensing and latching. For example, the integrators 411_b, 412_b, and 412_c integrate using the receiver reference clocks RClk1, RClk1_1st, and RClk1_2nd. Likewise, the sense and latch circuits 411_e, 412_h, and 412_i sense and latch using receiver reference clocks RClk1b, RClk1b_1st, and RClk1b_2nd simultaneously.

Multiplexer 415 is generating the output signal RX_D1 by receiving RX_D1_even and RX_D1_odd. Figure 4C is a block diagram of the second receiving circuit 420 shown in Figure 4A. We abbreviate the operating description of figure 4C because it is similar to figure 4B.

Figure 5 is a timing diagram of the receiver reference clocks as shown in Figures 4A-C. Referring to Figures 4A-C and 5, the receiver 404 includes two kinds of reference clocks: a full bit time clock and a half bit time reference clock. In one embodiment, clocks RClk1 and RClk1b, are full bit time clocks out of phase relative to each other. In one embodiment, clocks RClk1 and RClk1b are 180 degrees out of phase. In one embodiment, clocks RClk1_1st and RClk1_2nd, on the other hand, are half bit time clocks.

The half bit time clocks RClk1_1st and RClk1_2nd are generated from the full bit time reference clocks RClk1. In one embodiment, the bit time of the half bit reference clock RClk_1st is between 0 degrees and 90 degrees. In one embodiment, the bit time of the half bit reference clock RClk_2nd is between 90 degrees and 180 degrees.

The half bit time reference clocks RClk1b_1st and RClk1b_2nd are generated from the full bit time reference clocks RClk1b. In one embodiment, the bit time of the half bit reference clock RClk1b_1st is between 180 degrees and 270 degrees. In one embodiment, the bit time of the half bit reference clock RClk1b_2nd is between 270 degrees and 360 degrees.

The relationship between the full bit time reference clocks RClk2 and RClk2b and the half bit time reference clocks RClk2_1st, RClk2_2nd, RClk2b_1st, and RClk2b_2nd are similar to those described above with reference to RCLK1 and RCLK1b.

Figure 4c is a block diagram of the second receiving circuit 420 shown in Figure 4A.

The first and second receiving circuits 410 and 420 operate similarly.

Figure 6 is a timing diagram of the operation of the circuit 100 shown in Figures 1-6. Referring to Figures 1-6, the portion of the diagram marked G1 corresponds to timing associated with the transmitter 102 (202 in Figure 2A). The symbol data D1D2 is provided to the receiver 104 by the transmitter 102.

The G2 portion corresponds to timing associated with the receiving circuit 410 and the G3 portion corresponds to timing associated with the second receiving circuit 420. The inbound symbol data D1D2 is received by the receiving circuits 410 and 420 as, e.g., D1D2A and D1D2B. The timeslice T1 to T8 represents a full bit time relative to clocks RClk1 and RClk1b. Each symbol includes a full bit datum of TX_D1' and two half bit data of TX_D2'.

In the example of T3 of G2, the first receiving circuit 410 receives a symbol S2 of the symbol data D1D2A. The symbol S2 is one full bit datum of TX_D1' logic value high and two half bit data of TX_D2' logic value low and logic value high. The first receiving circuit 410 interprets the symbol S2 as one full bit datum of RX_D1_even' according to the RClk1, RClk1_1st, and RClk1_2nd.

In the example of T45 of G3, the second receiving circuit 420 receives a symbol S2 of the symbol data D1D2B. The symbol S2 is one full bit datum of TX_D2' logic value high and two half bit data of TX_D1' logic value high and logic value low. The second receiving circuit 420 interprets the symbol S2 as one full bit datum of RX_D2_odd' according to the clocks RClk2b, RClk2b_1st, and RClk2b_2nd.

In the example of T5 of G2, the first receiving circuit 410 receives a symbol S4 of the symbol data D1D2A. The symbol S4 is one full bit datum of TX_D1' logic value low and two half bit data of TX_D2' logic value high and logic value high. The first receiving circuit 410 interprets the symbol S4 as one full bit datum of RX_D1_even' according to the RClk1, RClk1_1st, and RClk1_2nd.

Figure 7 is a block diagram of a data transceiver equipped with an embodiment of the present invention. Referring to Figure 7, a semiconductor device 700 might be, e.g., a microprocessor, controller, memory device, or any other semiconductor device. The semiconductor device 700 comprises a data transceiver 701 capable of receiving and transmitting signals. The data transceiver includes a transmitter 702 and a receiver 704 commonly connected to a transmission line 706.

Figure 8 is a voltage level of the signals used in receiver 104 as we explained in more detail above.

Having illustrated and described the principles of our invention(s), it should be readily apparent to those skilled in the art that the invention(s) can be modified in arrangement and detail without departing from such principles. We claim all modifications coming within the spirit and scope of the accompanying claims.